DSD 2014

17th Euromicro Conference on
Digital System Design
Verona, Italy, August 27th-29th, 2014

Call for Papers

Scope

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of (embedded, pervasive and high-performance) digital and mixed hw/sw system engineering, covering the whole design trajectory from specification down to micro-architectures, digital circuits and VLSI implementations. It is a forum for researchers and engineers from academia and industry working on advanced investigations, developments and applications.

It focuses on today's and future challenges of advanced system architectures for embedded and high-performance hw/sw systems, application analysis and parallelization, design automation for all design levels, as well as, on modern implementation technologies from full custom in nanometer technology nodes, through FPGAs, to multi-core infrastructures. It covers a multitude of highly relevant design aspects from system, hardware and embedded-software specification, modeling, analysis, synthesis and validation, through system adaptability, security, dependability and fault tolerance, to system energy consumption minimization and multi-objective optimization.

Authors are kindly invited to submit their work according (but not limited) to the seven main topics of the conference main track. In addition, eight Special Sessions (with their own coordinators and subprogram committees) do also welcome contributions in specific themes of particular interest. All papers are reviewed following guidelines, quality requirements and thresholds that are common to all committees.

Main Topics

T1: (APP) Advanced applications of (embedded) digital systems.
T2: (AP-HwSw) Application analysis and parallelization for embedded and high-performance design.
T3: (SMVT) System, hardware and embedded-software specification, modeling, verification and test.
T4: (SHES) System, hardware and embedded software design and automatic synthesis.
T5: (SoC & NoC) Systems-on-a-chip and networks-on-a-chip.
T6: (RC) Programmable/re-configurable/adaptable architectures.
T7: (ET) Important issues introduced by emerging technologies.

Special Sessions/Organizers

SS1: (FDR) Flexible Digital Radio – *Dominique Noguet (CEA – Minatec, FR)*
SS2: (MSDA) Multicore Systems: Design and Applic.– *J. Sahuquillo (UPV Valencia, ES)- A. Molnos (CEA LETI, FR)*
SS3: (DTFT) Dependability, Testing and Fault Tolerance in Digital Systems – *H. Kubatova (CTU Prague, CZ) & Z. Kotasek (TU Brno, CZ)*
SS4: (ETCS) Emerging Technologies and Circuit Synthesis – *Tiziano Villa (U Verona, IT)*
SS5: (MCSDIA) Mixed Criticality System Design, Implementation and Analysis – *K. Grüttner (OFFIS, DE), E. Villar (TEISA U Cantabria, ES)*
SS6: (AHSA) Architectures and Hardware for Security Applications – *Paris Kitsos (TEI of Western Greece, GR)*
SS7: (DCPS) Design of Heterogeneous Cyber-Physical Systems – *Riccardo Muradore, University of Verona, Italy - Marc Geilen, Technical University Eindhoven, The Netherlands*
SS8: (EPDSD) European Projects in Digital System Design – *F. Leporati (U Pavia, IT), L. Jozwiak (TUE, NL)*

Submission Guidelines

Authors are encouraged to submit their manuscripts to http://www.easychair.org/conferences/?conf=dsd2014. Should an unexpected web access problem be encountered, please contact the Program Chair by email (DSD2014@unipv.it).

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the required IEEE format: single-spaced, double column, A4/US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the submitted manuscript, references included.

CPS, Conference Publishing Services, publishes the DSD Proceedings, available worldwide through the IEEE Xplore Digital Library. An extended version of the selected best papers will be published in a special issue of the ISI-indexed *"Microprocessors and Microsystems: Embedded Hardware Design"* Elsevier journal.

Important Dates

Deadline for paper submission: April 6th, 2014
Notification of acceptance: May 25th, 2014
Camera ready papers: June 15th, 2014

More Information (web pages)

- **DSD 2014: *http://www.euromicro.org/dsd/***
- **Euromicro: *http://www.euromicro.org***

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MAIN TOPICS DESCRIPTION

T1: Advanced applications of (embedded) digital systems
Challenging and highly-demanding modern applications in (wireless) communication and networking; networked electronic media, multimedia and ambient intelligence; image and video processing; mobile systems; health-care and medicine; ubiquitous, wearable and implanted systems; military, space, avionics, measurement, control and automotive applications; wireless sensor network applications; surveillance and security; environmental, agriculture, urban, building, transportation, traffic, energy, hazards and disasters monitoring and control.

T2: Application analysis and parallelization for embedded and high-performance hardware and software design
Application profiling, characterization and bottleneck detection; application re-structuring to reveal parallelism; application parallelization, information-flow analysis, scheduling and mapping for application-specific processor and MPSoC memory and communication architecture synthesis; hw/sw co-design and algorithm/architecture matching; combined hardware/software design space exploration and hw/sw system multi-objective optimization; parallelization, scheduling and mapping of applications for (heterogeneous) processor and MPSoC architectures; re-targetable (application-specific) compilation; architectural support for compilers/programming models; performance, energy consumption and other parametric analysis for HW/SF systems; analytical modeling and simulation tools; benchmark applications, workload and benchmarking for heterogeneous hw/sw systems; virtual and FPGA-based system prototyping.

T3: System, hardware and embedded-software specification, modeling, verification and test
Modeling, simulation, design and verification languages; functional, structural and parametric specification and modeling; model-based design and verification; system, hardware, and embedded software analysis, simulation, emulation, prototyping, formal verification, design-for-test and testing at all design levels; dependability, safety, security and fault-tolerance issues.

T4: System, hardware and embedded software design and automatic synthesis
Quality-driven design; model-, platform- and template-based design; design-space exploration; multi-objective optimization; system, processor, memory and communication architecture design; application scheduling and mapping to platforms; application-specific circuits and processors; arithmetic, signal, vector and graphics processing units; hardware accelerators; transaction level modeling and higher-level modeling; synthesis of asynchronous and dataflow systems; methods and CAD tools for analysis and synthesis of systems, architectures, embedded and high-performance software, and hardware at high-, logic- and physical level; methods and CAD tools for modeling, analysis and optimization of performance, energy consumption, reliability, robustness, safety, security, and testability.

T5: Systems-on-a-chip and networks-on-a-chip
(Heterogeneous) multiprocessor systems on-a-chip (MPSoC), hardware multiprocessors and complex accelerators; generic system platforms and platform-based design; processor, memory and communication architectures; 3D MPSoCs and 3D NoCs; ASIP, GPU and cell-based platforms; software design and programming models for multicore platforms; IP design, standardization and reuse; parallelism exploitation and scalability techniques; virtual components; system of systems; compiler assisted MPSoCs; hardware support for embedded kernels; embedded software features; static, run-time and dynamic optimizations of embedded MPSoCs; benchmarks and benchmarking for MPSoCs; NoC architectures, quality of service in NoCs; power dissipation and energy issues in SoCs and NoCs.

T6: Programmable/re-configurable/adaptable architectures
Design methodologies and tools for reconfigurable computing; run-time, partial and dynamic reconfiguration; fine-grained, mixed-grained and coarse-grained reconfigurable architectures; reconfigurable interconnections and NoCs; FPGAs; systems on re-configurable chip; system FPGAs, structured ASICs; co-processors; processing arrays; programmable fabrics; adaptive computing devices, systems and software; adaptable ASIPs and ASIP-based MPSoCs; hardware accelerators; optimization of FPGA-based cores; shared resource management; novel models, design algorithms and tools for FPGAs and FPGA-based systems; rapid prototyping systems and platforms; adaptable wireless and mobile systems.

T7: Emerging technologies
Important issues for the system, circuit and embedded software design introduced by e.g. the nanometer CMOS and beyond CMOS technologies, 3D integration, optical and other new memory and communication technologies; new human-machine interfaces, neural- and bio-computation, (bio)sensor and sensor network technologies, pervasive and ubiquitous computing, "internet of things"; related design methods and EDA tools.

SPECIAL SESSIONS

In addition to the above Main Topics (the Conference “traditional core”), papers are also sought for the special sessions SS1 - SS8. Prospective authors are invited to submit papers related to design methodologies and architectures for multi-standard, multi-mode flexible radios (SS1), performance improvement and energy consumption reduction for multicore systems (SS2), system and SoC dependability and testing (SS3), new techniques and tools for logic synthesis, physical design and testing of circuits in emerging technologies (SS4), integration of multiple functions with different criticality and certification assurance levels (SS5), architectures and hardware for secure embedded systems, e.g. smart cards, DSPs, RFID and Wireless Sensor Networks, hardware Trojans – insertion/detection methodologies, side channel analysis (SS6), heterogeneous distributed pervasive networked embedded and cyber-physical systems (SS7), issues and solutions researched in just started, ongoing or recently finished European Projects of FP7, Artemis, Eniac, Medea+ etc. in the (embedded, pervasive and high-performance) Digital System Design Area (SS8).